International Journal of Management, IT & Engineering
Vol. 9 Issue 4, April 2019,
ISSN: 2249-0558 Impact Factor: 7.119
Journal Homepage: http://www.ijmra.us, Email: editorijmie@gmail.com
Double-Blind Peer Reviewed Refereed Open Access International Journal - Included in the International Serial Directories Indexed & Listed at: Ulrich's Periodicals Directory ©, U.S.A., Open J-Gage as well as in Cabell's Directories of Publishing Opportunities, U.S.A

Power Gating technique for leakage Power Reduction in Sequential Circuit

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***Abstract*—Portable and hand-held devices are significant now a days. So, leakage power reduction has emerged as the primary concern of today's VLSI designers. This leads to the concept of power gating methods to reduce the leakage power. Subclock (SCPG) and Stacking methods of power gating techniques are employed to reduce leakage power in the literature. To attain a better leakage power and improved peak power values, here a modified Subclock (MSCPG) method of power gating is proposed. The proposed method has 1bit Comparator for combinational circuit and D flip-flop for sequential circuit. The performance of the MSCPG method is analyzed in a sequential 4 bit SISO (Serial in Serial out circuit) using Cadence 180nm technology tool. The MSCPG method shows an improved performance than the other power gating methods.**

Index Terms—Subclock, Stacking, Modified Subclock power gating, Isolate design, Sleep transistor,Shift register, SISO.

I. INTRODUCTION

The drastic improvement in the field of semiconductor technology leads to a progressive improvement in the performance of portable systems accompanying intensified reliability. The battery power available is limited in portable applications and hence it is essential to reduce leakage power consumption. [1]. consequently, the top priority issue for VLSI circuit design is being recognized as leakage power dissipation. Leakage power makes up to 45% of the total power consumption in today's high performance microprocessors [2]. Therefore low power design plays a key role in leakage power reduction. There are different schemes to reduce leakage power dissipation like stacking and Subclock power gating.

In this paper, a new method, called Modified sub clock power gating (MSCPG) has been proposed, to improve the leakage and peak power reduction. The proposed MSCPG technique is analyzed in 4 bit SISO. In addition, the proposed MSCPG is compared with various Subclock and Stacking methods in 4 bit SISO. The comparison results shows the proposed technique have better leakage and peak power reduction. The proposed MSCPG method can be used in applications like microprocessor, multicore CPU, cmos circuits and FPGA.

II. POWER GATING SCHEMES FOR LEAKAGE POWER REDUCTION

In the idle circuit blocks power gating is an effective approach for minimizing the leakage power. It is called as MTCMOS (Multi Threshold CMOS). Here the addition of sleep transistor is made above and below the combinational logic. The sleep transistor is used to control the gate's access to the power supply, the gated power supply is known as virtual VDD. Suppose gate uses low threshold transistor it increases gate delay and increase leakage current. For minimizing the leakage has high threshold voltage (Vth) sleep switches are used [2].

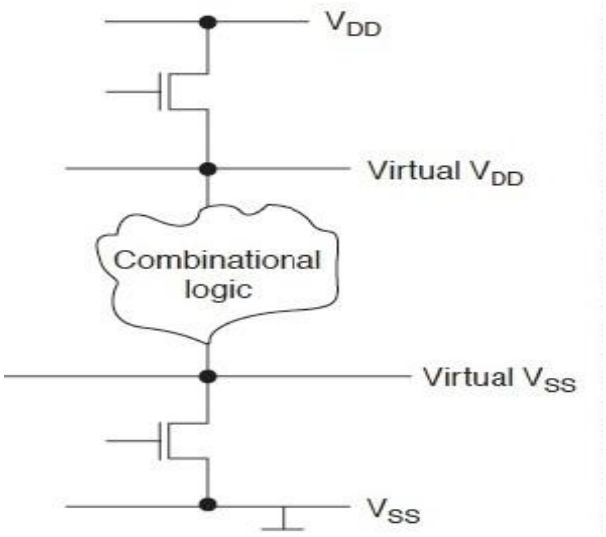

Fig.1 Structure of Power gating

Power gating has the basic strategy of providing two power modes:

- Sleep mode
- Active mode

Switching between the above two modes at the appropriate times and manner is the best goal to improve power saving performance. Two sleep transistors namely header switch and footer switch are used.

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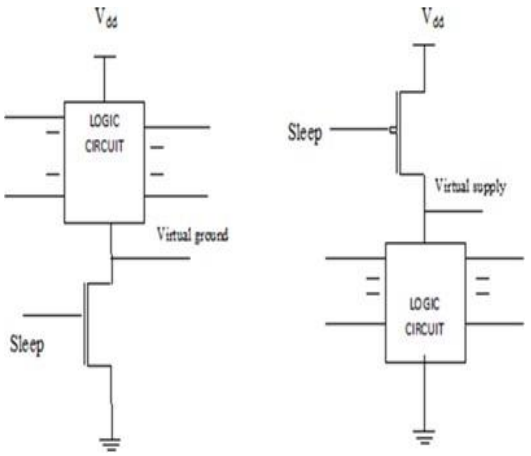

Fig.2 Header switch and Footer switch implementation in logic blocks

The PMOS transistor is used to implement the header switch. The power supply is controlled by the header transistor switch. PMOS devices tend to exhibit lower gate leakage than NMOS, so using header sleep devices lowers the gate leakage. A header switch has to achieve the same resistance in linear region. So PMOS must be greater than NMOS. To control V_{SS} supply NMOS transistor is used as a footer switch. In the existing system has two methods were analyzed. They are

i) Stacking power gating
ii) Sub clock power gating

A. STACKING POWER GATING

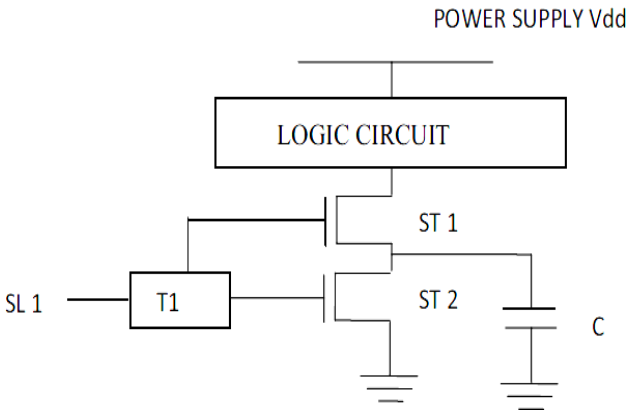

Fig.3 Stacking power gating

Reduction in leakage current is achieved with the help of stacking effect; this in turn reduces the leakage power in which sleep transistors are used to reduce the current peak and voltage glitches. And also reduce the Ground bounces reduction by tuning the voltage at the transitional node level [2].

The advantage of stacking scheme is to reduce the leakage power, peak power, and leakage current [9].

i) Leakage current reduction

During the sleep mode when both ST1 and ST2 sleep transistors are turned OFF, it swings in-between the node voltage VGN1 and VGN2 to positive values due to small drain current. The stacking scheme reduces the peak current and voltage glitches in power rails. When the intermediate node voltage VGN becomes positive due to small drain current by switching off the sleep transistors (ST1and ST2). It has four major effects are:-

1. Gate source voltage *(*Vgs1*)* becomes negative.
2. Negative body to supply voltage *(*Vbs1*)* causes more body effect.
3. Drain to source voltage *(*Vds1*)* of ST1 (sleep transistor) was decreased, which results minimizing the drain induced barrier lowering.
4. The Drain-source voltage *(*Vds2*)* is of ST2 is less compared to ST1, because most of the voltage drop across ST1 is in sleep mode. This reduced the drain induced barrier lowering [11].

ii) Drain induced barrier lowering(DIBL)

The DIBL is the lowering of energy barrier between the channel and source. These causes excess injection of source's potential barrier to be lowered in the channel and increase the Sub-threshold.

The Sub-threshold current is a function of the threshold voltage (Vt). The flowing of current through a series connection of stacked transistors reduces when more than one transistor in the stack is turned off. This effect is known as stacking effect. The resistance path are reduced during the active mode transistor are turned on [8].

B. SUBCLOCK POWER GATING

The sub-clock methodology is used as reducing the leakage power. This sub-clock power gating scheme used to optimize the power consumption for the IDLE mode operation in active mode condition. The sub-clock power gating method to check the clock period and to reduce multiplex clock cycles in a new approach, called sub-clock power gating [1].

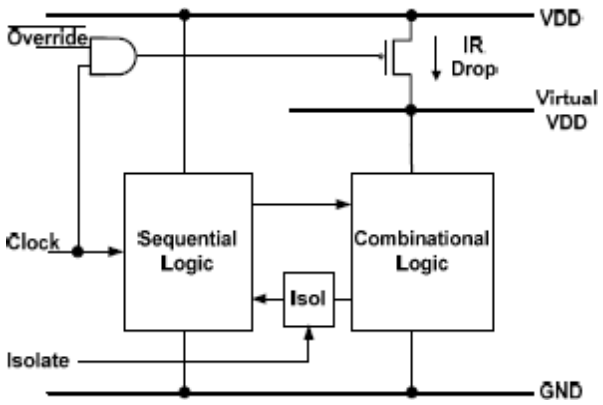

Fig.4 Subclock power gating

In the Subclock power gating has combinational, sequential and Isolation block are there. The combinational logic is constructed by the 1 bit comparator circuit and the sequential logic is constructed by D flip flop circuit. The significant reduction in leakage power is achieved by using the power gating method.

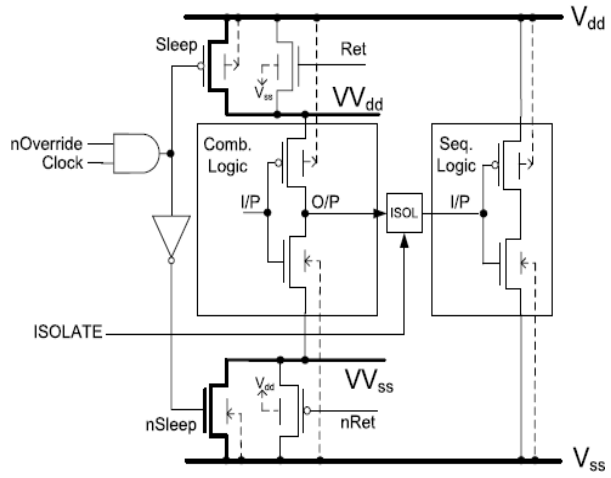

Fig 5 Sub clock power gating with symmetric virtual rail clamping

The above fig 5 shows symmetric virtual rail clamping is added to the above and below the inverter circuit. The NMOS and PMOS transistors at the head of the combinational logic (Sleep and Ret) use the normal clock signal while the nmos and pmos transistor switches at the foot (nSleep and nRet) use the reverse of the clock signal. Therefore, when the clock is high, the combinatorial logic is clamped to less than Vth by the symmetric virtual rail clamping and when the clock is low it is restored to Vdd [7].

i) Isolation circuit

The isolation circuit should be inserted between powered down and powered up modules and all inputs of powered up modules are connected to appropriate voltage levels. Isolation circuits can be attached to the outputs of powered down modules or powered up modules.

The circuit has three inputs: the clock signal, the value of the combinational logic VVdd that is derived from a TIEHI logic gate, and the noverride signal. When the clock is logic 1, ISOLATE is driven to logic 1, thereby separating the combinational outputs.

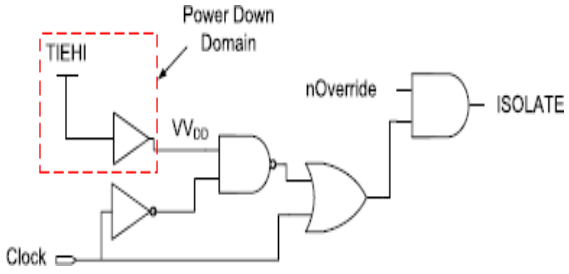

Fig.6 Isolation circuit

When the clock is logic 0, ISOLATE is held at logic 1 while the VVdd input remains at logic 0 (clamped). This ensures the combinational outputs remain isolated until the source rail is charged to an equivalent logic 1, eliminating short-circuit currents during wake-up.

III. MODIFIED SUBCLOCK POWER GATING METHOD

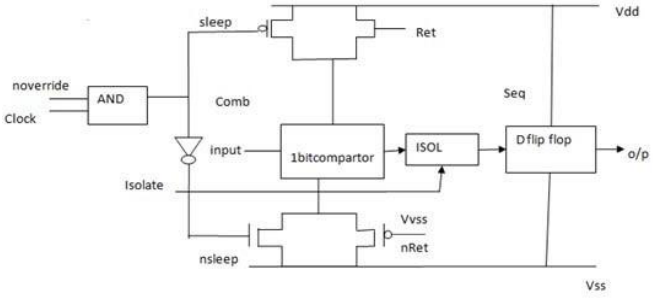

Fig.7 Modified Subclock power gating

The modified Subclock power gating consists of 1 bit comparator, D flip flop and Isolation. The 1bit magnitude comparator is a power gatable combinational logic. In this the symmetric virtual rail clamping is added to above and below of the comparator circuit. The symmetric virtual clamping for maintaining the voltage level in the comparator device circuit [1].

i) *1 Bit comparator*

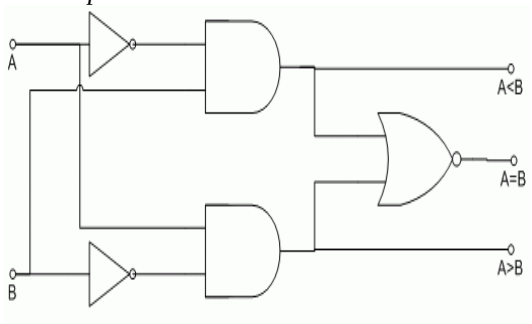

Fig. 8 1 bit comparator gate level diagram

The 1 bit comparator gate level diagram consists of two inputs and three outputs. A magnitude comparator is a hardware based device and also a combinational logic circuit that compares two given numbers and determines whether one is equal to, less than or greater than the other.

ii) *Applications of comparator*

- The comparator finds the application in the field of address decoding circuit in computer and microprocessor based devices to select input and output devices for data storage.
- The servo motor control and process controllers using the magnitude comparator.

iii) *D flip flop*

The D flip flops are designed from a gated SR flip flop with a complementary circuit added in between the S and the R inputs to for permitting a single D (data) input. This data input D is applied to "set" the signal, whereas its complement is applied to generate the "reset" signal resulting in level-sensitization of D flip-flop from a level-sensitive RS-latch as now S = D and R not D .The D flip flop perceives the designation from its ability to transfer “data” into a flipflop. It is also expanded as Delay Flip Flop.

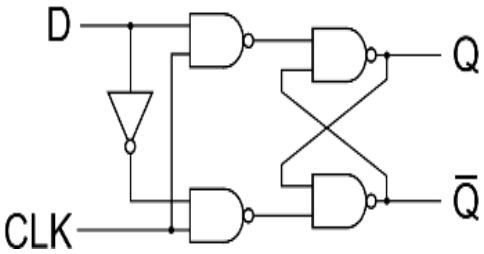

Fig.9 D Flip flop block

Fig.9 shows the alternation of basic clocked SR flip flop that results in D flipflop. The D flip-flop is the most significant among the clocked flip-flops as it make sure that inputs S and R are never equal to one at the simultaneously. It consists of one inverter and four NAND gates are there. The data and clock is given to the input of Inverter and NAND gate. The output is produced as Q and Q bar.

iv) *Application of D flipflop*

- Some parts of digital systems operate at a slower rate than the clock. (Serial Input and Output, Analog and Digital conversion, etc).
- Flip-flops can be used to split the masterly clock frequency into slower clock cycles for above applications.
- The flip flops are used in digital counters − Digital counters not only count things, but are useful as frequency meters, parts of A/D converters, etc.

IV. 4 BIT SISO USING MODIFIED SUBCLOCK POWER GATING

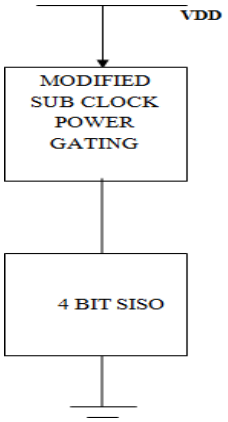

Fig.10 Modified SCPG with SISO

The proposed MSCPG is analyzed in 4 bit SISO for reducing leakage and Peak power. The modified Subclock power gating is linked between source supply and SISO. The power reduction is attained by using modified power gating.

For analyzing the leakage power modified Subclock power gating with shift register is used. The Sequential logic is a Shift register that can be used for stores or moves of data in the form of binary numbers. This sequential logic loads the present data on its inputs and then shifts through its output once each clock cycle. So this is named as Shift Register.

Shift Registers are worn for storage and movement of data. It is commonly used inside calculators, computers to store data such as two binary numbers previously they are added together, or to convert the data from serial to parallel or parallel to serial data format. The individual data latches that generate a single shift register are all directed by a common clock (Clk) signal called synchronous device [5].

i) 4 Bit serial in serial out shift register

The data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control. In the 4 bit (SISO) shift register has, when the clock signal is applied and the serial data is given; only one bit will be possible at output at a moment in the order of the input data. The uses of SISO shift register is to deed as temporary data storage device. However the main use of a SISO is to act as a delay element.

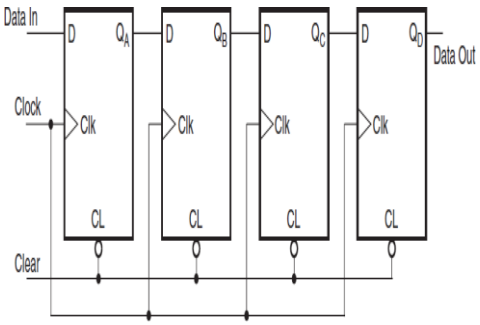

Fig.11 4bit serial in serial out shift register block

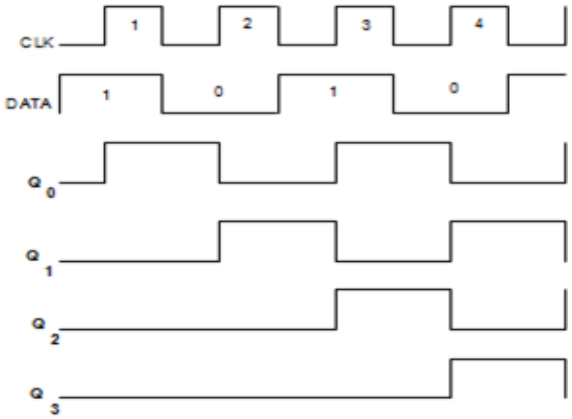

Fig.12 4 bit SISO output waveform

The first clock transition, the QA output goes from logic ‘0’ to logic ‘1’. The outputs of the other three flip-flops

remain in the logic '0' state as their D inputs were in the logic'0' state at the time of clock transition. During the second clock transition, the QA output goes from logic '1' to logic '0' and the QB output goes from logic '0' to logic '1', again in accordance with the logic status of D input at the time of relevant clock transition.

Thus the 4 bit SISO shift register, it takes four clock cycles to load the data bits and another four cycles to read the data bits out of the register.

V. SIMULATION RESULTS

The power gating methods are analyzed in 4 bit SISO sequential circuit and their performances in terms of leakage power reduction and peak power values are evaluated. The performances of power gating approaches are simulated using cadence window in CADENCE 6.1.5 software.

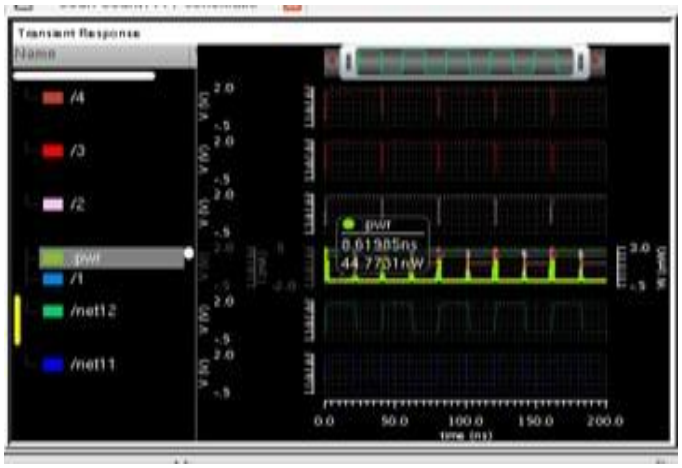

Fig.13 Leakage power waveforms of 4 bit serial in serial out shift register

The Fig.13 shows the simulation waveform for 4 bit SISO. From the waveform the observed leakage power value of SISO is 44.77nW.

Fig.14 Simulation of Leakage power waveforms 4 bit serial in serial out shift register with stacking power gating

The Fig.14 shows the simulation waveform for 4 bit SISO with stacking power gating. From the waveform the observed leakage power value of SISO with stacking power gating is 41.32nW.

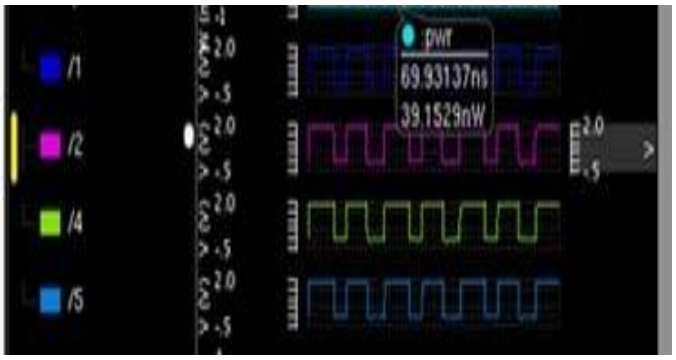

Fig.15 Simulation waveform for sub clock power gating with 4 bit serial in serial out shift register

The Fig.15 shows the simulation waveform for sub clock power gating with 4 bit SISO. From the waveform the observed leakage power value of SISO with SCPG is 39.15nW.

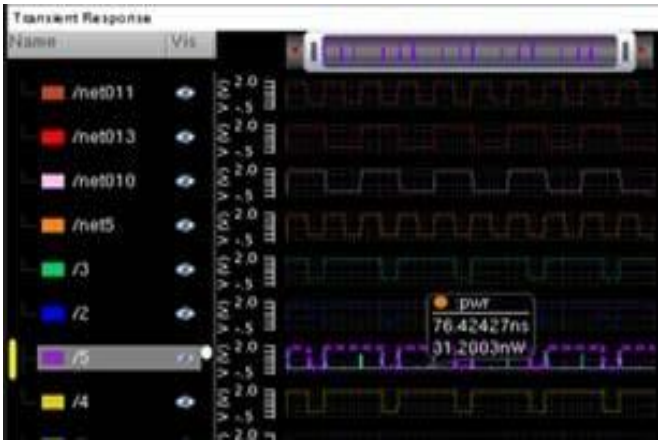

Fig.16 Simulation waveform for Leakage power in Modified SCPG with 4 bit serial in serial out shift register

The Fig.16 shows the simulation waveform for 4 bit SISO with MSCPG. From the waveform the observed leakage power value of SISO with MSCPG is 31.20nW.

TABLE I
i)PERFORMANCE EVALUATION OF POWER GATING METHODS

PARAMETERS	SISO			
	WITHOUT POWER GATING	WITH POWER GATING		
		STACKING POWER GATING	SUB CLOCK POWER GATING	MODIFIED SUB CLOCK POWER GATING
LEAKAGE POWER	44.77nW	41.32nW	39.15nW	31.42nW
PEAK POWER	0.1839W	0.099W	0.096W	0.049W

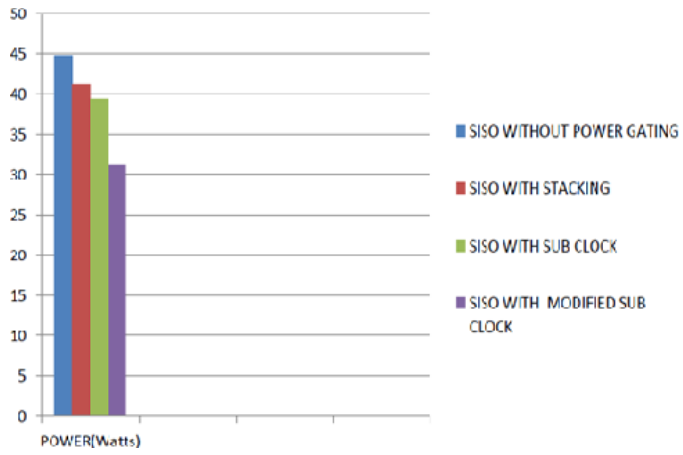

Fig. 17 Leakage power for SISO with and without power gating

Table I and fig.17 shows the leakage power and peak power values for 4 bit Serial in serial out shift register using Stacking power gating, Subclock power gating and modified Subclock power gating methods. The proposed modified Subclock power gating achieves 13% improved leakage power reduction and 12.5% improved peak power values compared with Stacking power gating and Subclock power gating.

VI. CONCLUSION

The primary concern in VLSI design is to reduce the leakage power dissipation. Power gating design provides significant contraction leakage power results. In this paper, different power gating such as Stacking power gating, Subclock power gating were analyzed for leakage(static) power reduction and a modified Subclock power gating was proposed for improvement of leakage power reduction. Simulation results using Cadence for modified Subclock power gating shows a 13% significant improvement in leakage power reduction and 12.5% improvement in peak power values when compared with other power gating schemes. Perhaps the proposed (MSCPG) used to meet the challenges in all portable devices, communication devices and microprocessors. In future, modified Subclock power gating technique can be analyzed for low power applications too.

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